

**IN THE SPECIFICATION**

Please amend the Abstract on page 52 of the application as follows:

A data processor includes execution clusters, an instruction cache, an instruction issue unit, and alignment and dispersal circuitry. Each of the execution clusters includes an instruction execution pipeline. Each execution pipeline has a number of processing stages, and each execution pipeline is a number of lanes wide. The processing stages are used to execute instruction bundles, where each instruction bundle has one or more syllables. Each of the lanes is capable of receiving one of the syllables of an instruction bundle. The instruction cache includes a number of cache lines. The instruction issue unit receives fetched cache lines and issues complete instruction bundles toward the execution clusters. The alignment and dispersal circuitry receives the complete instruction bundles from the instruction issue unit and routes each of the received complete instruction bundles to a correct one of the execution clusters. The complete instruction bundles are routed as a function of at least one address bit associated with each of the complete instruction bundles.

~~There is disclosed bundle alignment and dispersal circuitry for use in a data processor. The data processor comprises: 1) C execution clusters, each of the C execution clusters comprising an instruction execution pipeline having N processing stages for executing instruction bundles comprising from one to S syllables, wherein each the instruction execution pipelines is L lanes wide, each of the L lanes for receiving one of the one to S syllables of the instruction bundles; 2) an instruction cache for storing a plurality of cache lines, each of the~~

~~cache lines comprising C\*L syllables; 3) an instruction issue unit for receiving fetched ones of the plurality of cache lines and issuing complete instruction bundles toward the C execution clusters; and 4) alignment and dispersal circuitry for receiving the complete instruction bundles from the instruction issue unit and routing each the received complete instruction bundles to a correct one of the C execution clusters as a function of at least one address bit associated with each of the complete instruction bundles.~~